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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,080	03/07/2001	Natalino Giorgio Busa	NL000133	5082

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,080	BUSA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) *6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-5 are presented for examination. Clams 6-7 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by McNeill et al. (4,876,643).

3. As to claims 1,4, McNeill teaches a system (see fig.2, see also fig.3) comprising a master controller [210], a first functional unit (see group of 212s) including a slave controller [212] a second functional unit (see the disk manger 16, 22 in fig.1), and a common memory (see shared memory 214) shared by the first and second functional units, the device being programmed for executing an instruction by the first functional unit (see the programmed slave processor 212 in col.6, lines 55-61), the execution of involves I/O operations by the first functional unit (see the disk interface in col.7, lines 36-40), where the execution involves al least one of output data (see the search pattern match , see also col.6, lines 65-68, col.7, lines 20-35) of the first functional unit expressed by the second functional unit (see the indexed files in col.3, lines 15-21) in the midst of execution of the instruction (see the command from master for search

assignment in col.7, lines 1-20, see also col.4, lines 35-41, see fig.7) and the input data to the first functional unit being generated by the second functional unit of the instruction (see how the master mange communication between the input streams in col;.6, lines 39-54) .

4. As to claim 2, McNeill also included relative latency (see wait time in col.7, lines 5-20).

5. As to claims 3,5, McNeill also included a halt means (see the wait for next record and list in col.7, lines 2-35).

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Connor (6,266,766).

7. As to claim 1, O'Connor discloses a data processing device, comprising a master controller, a first function unit (see fig.1 [10]) including a slave controller, a second function unit (see fig.1 [20]), and a common memory shared by the first and second functional units (see fig. 1 [30]), the data processing device being programmed for executing an instruction, execution of the instruction involving I/O operations by the first functional unit, wherein said

execution involves at least one of output data of the first functional unit being processed by the second function unit in the of execution of the instruction and input the input data to the first function unit being generated by the second functional unit in the midst of execution of said instruction. (see col. 1 , lines 16-17 and lines 28-32, see the execution of instructions), the first execution unit outputs data processed by the second function unit and data input to the first function unit by the second function unit (see fig.1) during execution because the data is then executed by the execution units. As to the language of "in the midst of " execution of that instruction, It is read as in close range, therefore a functional unit operating in the midst of execution by another functional unit is only operating in time close to another function unit which encompasses sequential , concurrent and any type of processing. Therefore when the second execution unit executes data directly given from the first execution unit (see fig.1) , the operation of the second execution unit is in close range to the execution of the first execution unit and operates in the midst of the execution of the first unit. O'Connor also taught that the processor uses interlocks when data is not ready (see Col.1, lines 32-53) . It can be seen that bypassing eliminates some need for interlocking, but an interlock is needed for the data which has not been executed and ready for bypassing. Therefore, interlocking exists in the processor and a master controller must have the control of the interlocks (see col. 2, lines 9-10 and fig. 2 , see the separate controller for controlling the bypass functionality , see the slave controller).

8. As to claim 2, O'Connor teaches the first function unit is arranged for processing instructions of a first type corresponding to operations having a relatively

large latency and the second function unit is arranged for processing instructions of a second type corresponding to operations having a relatively small latency. O'Connor discloses each of the execution units take varying amounts of time to complete (see col. 1, lines 54-61). Therefore, the first functional unit takes longer than the second. And, the first function unit processes operations of a relatively large delay and the second function unit of a relatively small delay .

9. As to claim 3, O'Connor discloses halt means controllable by the master controller for suspending operation of the first functional unit. The master controller is used for implementing interlocks, which is halting or suspending execution if the data is not ready. Therefore, the first function unit is halted when the data is not .

10. As to claim 4, O'Connor discloses a method of operating a data processing device, comprising'.

a) a master controller for controlling operation of the data processing device;

(e.g. see col. 1, lines 32-53 , see the interlocks when data is not ready). An interlock is needed if the data not been executed and ready for bypassing. Therefore, interlocking exists in the processor and there must be a master controller to control the interlocks.

b) a first function unit, which includes a slave controller (see (figure 1, [10] for the first unit), the first function unit [10] being arranged for executing instructions of a first type corresponding to operations having a relatively long latency; (see col. 1,

lines 16-17 and lines 28-32 , see the execution of instructions. Col. 2, lines 9-10 and figure 2 show that there is a separate controller for controlling the bypass functionality. This is the slave controller. The execution units take varying amounts of time to complete (see col. 1 , lines 54-61, see different types of instructions). Therefore, the first function unit takes longer than the second. And, the first function unit processes operations of a relatively large delay.

c) a second function unit capable of executing instructions of a second type corresponding to operations having a relatively short delay (see fig.1, [20]), wherein the first function unit during execution of an instruction of the first type receives input data and provides output data, and the execution involves at least one of: output data of the first functional unit being processed by the second functional unit in the midst of execution of said instruction and input data to the first functional unit being generated by the second functional unit in execution of the instruction. The first function unit has a relatively long delay compared to the second unit so the second function unit has a relatively shod latency. The second function unit provides input data for the first function unit and receives output data from the first unit (see fig.1). This is done during execution because the data is then executed by the execution units. As to the language "in the midst of " , it is read as I the close range of . Therefore, a functional unit operating in the close range of execution by other function unit is only operating in time proximate to the other function unit and encompasses all type of processing, such as sequential, concurrent, and other processing. O'Connor teaches the second execution unit executes data directly given from the first execution unit, the operation of the second

execution unit is in close range to the execution of the first execution unit and therefore, operates in the midst of the execution of the first unit.

11. As to claim 5, O'Connor also discloses his master controller temporarily suspends operation of the first functional unit during execution of instructions of the first type. The master controller is used for implementing interlocks , halting , or suspending execution, if the data is not ready. The first functional unit is halted when data is not ready.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Yasuda is cited for the teaching of master/slave control of a plurality of functional units the (see fig.3, col.6, lines 3-68, col.7, lines 1- 37).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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